

PATENT NUMBER

**U.S. UTILITY** Patent Application

2/15

**O.I.P.E.**

PATENT DATE

**SCANNED**

**Q.A**

APPLICATION NO.  
09/551027

CONT/PRIOR  
D

**CLASS**

SUBCLASS

ART UNIT

EXAMINER

## APPLICANTS

Wendell Noble  
Leonard Forbes

### Title

Circuit and method for a folded bit line memory cell with vertical transistor and trench capacitor

PTO-2040  
12/99

# CPA

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<div style="border: 1px solid black; padding: 2px; display: inline-block; margin-bottom: 5px;"> </div> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			<b>NOTICE OF ALLOWANCE MAILED</b>	
<input checked="" type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. <u>6,156,604</u> <u>6,156,607</u>	_____ (Primary Examiner) (Date)			<b>ISSUE FEE</b>	
				Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) (Date)			<b>ISSUE BATCH NUMBER</b>	
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